



U.S. DEPARTMENT OF COMMERCE
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LIST OF ART CITED BY APPLICANT
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U.S. PATENT DOCUMENTS

EXAMINER NAME	Document Number	Date	Name	Class	Subclass	Filing Date If Applicable
KAD	6,518,422	03/03	Chen, et al	438	257	
KAD	6,492,488	12/02	Ng (U.G.)	257	360	
KAD	6,373,154	04/01	Jeng, et al	257	413	
KAD	20010018668	09/01	Gonzales, et al	438	275	
KAD	6,583,518 B1	03/03	Jeng	438	584	
KAD	6,485,061 B1	11/02	Xia, et al	438	680	
KAD	6,486,057 B1	11/02	Yeh, et al	438	633	
KAD	6,485,372 B1	10/02	Xia, et al	438	787	
KAD	6,484,593 B1	05/02	Ngo, et al	438	788	
KAD	6,436,808 B1	06/01	Ngo, et al	438	623	
KAD	6,435,943 B1	05/01	Cheng, et al	438	28	
KAD	6,429,145 B1	05/02	Tsai, et al	438	622	
KAD	6,384,677 B1	09/01	Wu, et al	438	783	
KAD	6,030,908	01/08	Hopper, et al	438	711	

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translators
				Yes	No	
KAD	8046186	01/96	JP	—	—	abstract
KAD	8046188	01/96	JP	—	—	abstract
KAD	7501726	05/95	JP	—	—	abstract
KAD	6132113	05/94	JP	—	—	abstract

OTHER REFERENCES (including Author, Title, Date, Reference Page, etc.)

KAD	AR	Wolf, S. "Silicon Processing for the VLSI Era", Vol. 1, pp. 403-413.
KAD	AS	Wolf, S. "Silicon Processing for the VLSI Era", Vol. 2, pp. 48-49 and 415.

EXAMINER *K. Duda*

DATE CONSIDERED

2-19-04

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09881385APPLICANT
Michael Hukker et al.FILING DATE
Jan 15, 2001GROUP
156

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JKD	5,133,615	10/90	Shriver	257	646	
JKD	5,984,217	11/99	Ng	438	636	
JKD	5,885,519	11/99	Kakimoto et al.	430	313	
JKD	5,347,385	03/98	Kurose et al.	438	723	
JKD	5,829,687	06/97	Roman et al.	438	69	
KMD	5,495,535	05/96	Li et al.	438	302	
KMD	5,891,000/044	06/91	OMA	438	687	
KMD	5,801,604/311	06/93	Cheng et al.	438	704	
AK						
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FOREIGN PATENT DOCUMENTS

Document Number	Date	Country	Class	Subclass	Translation	
			Yes	No		
AM						
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AP						

OTHER REFERENCES (including Author, Title, Date, Page, etc.)

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